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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/735,479	12/14/2000	Kenichi Watanabe	001620	8362

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ARMSTRONG, WESTERMAN, HATTORI,
McLELAND & NAUGHTON
Suite 1000
1725 K Street, N.W.
Washington, DC 20006

EXAMINER
PERALTA, GINETTE

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/735,479	WATANABE ET AL.	
	Examin r	Art Unit	
	Ginette Peralta	2814	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-7 and 19-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7 and 19-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uglow et al. in view of Huang et al. (U. S. Pat. 6,060,379).

Uglow et al. teaches in Fig. 10B a semiconductor device that comprises an underlie 100 having a conductive region 122 in a surface layer of the underlie 100; an insulating etch stopper film 102′ covering a surface of the underlie 100; an interlayer insulating film (104′-106′) formed on the insulating etch stopper film 102′; a wiring trench formed in the interlayer insulating film, the wiring trench having a first depth from a surface of the interlayer insulating film; a contact hole extending from a bottom surface of the wiring trench to a surface of the conductive region through a remaining thickness of the interlayer insulating film and through the insulating etch stopper film 102′; and a dual damascene wiring layer 302 embedded in the wiring trench and in the contact hole; wherein the interlayer insulating film includes a first kind of insulating layer 106′ surrounding a side wall and the bottom surface of the wiring trench and a second kind of insulating layer 104′ disposed under the first kind of the insulating layer

106′ and having etching characteristics different from the first kind of the insulating layer.

Uglow et al. teaches all the limitations in the claim with the exception of the contact hole having a portion whose cross sectional area gradually increases toward an upper level in the first kind of insulating layer.

Huang et al. discloses in Figs. 1E, 2E, and 5E, a semiconductor device that includes an underlie having a conductive region in a surface layer of the underlie; an interlayer insulating film formed on the surface; a wiring trench formed in the interlayer insulating film, the wiring trench having a bottom surface at a first depth from a surface of the interlayer insulating film and a side wall; a contact hole extending from the bottom surface of the wiring trench to a surface of the conductive region through a remaining thickness of the interlayer insulating film; wherein the contact hole has an upper portion whose cross sectional area gradually increases toward an upper level and reaches the bottom surface o f the wiring trench in the insulating layer (fig. 1E), wherein the structure is a conventional dual damascene structure and where the gradual increase of the contact hole aids in the deposition of a conformal barrier layer that enhances the adhesion of the embedded conductive layer while preventing the diffusion of the embedded layer.

Thus, it would have been obvious to one of ordinary skill in the art to use a contact hole having a gradual increase toward an upper level as Huang et al. teaches that this is well known and conventional in the art, and an inherent result of the gradual

increase is a conformal barrier layer that aids in the adhesion of the embedded conductive layer while preventing the diffusion of the embedded layer.

Regarding claim 7, Uglow further teaches the second kind of the insulating layer 104′ being disposed on the insulating etch stopper 102′ and has a thickness thinner than the first depth.

3. Claims 3-6, and 19-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uglow et al. in view of Huang et al. and further in view of Tsai et al. (U. S. Pat. 6,319,814 B1).

Regarding claims 3 and 6, Uglow et al., as modified by Huang et al. above, teaches in Fig. 10B a semiconductor device that comprises an underlie 100 having a conductive region 122 in a surface layer of the underlie 100; an insulating etch stopper film 102′ covering a surface of the underlie 100; an interlayer insulating film (104′-106′) formed on the insulating etch stopper film 102′; a wiring trench formed in the interlayer insulating film, the wiring trench having a first depth from a surface of the interlayer insulating film; a contact hole extending from a bottom surface of the wiring trench to a surface of the conductive region through a remaining thickness of the interlayer insulating film and through the insulating etch stopper film 102′; wherein the contact hole has an upper portion whose cross sectional area gradually increases toward an upper level and reaches the bottom surface o f the wiring trench in the insulating layer (Huang's fig. 1E); and a dual damascene wiring layer 302 embedded in the wiring trench and in the contact hole; wherein the interlayer insulating film includes a first

kind of insulating layer 106′ surrounding a side wall and the bottom surface of the wiring trench and a second kind of insulating layer 104′ disposed under the first kind of the insulating layer 106′ and having etching characteristics different from the first kind of the insulating layer.

Uglow et al., as modified by Huang et al. teaches all the limitations in the claims, further including the use of fluorosilicate glass (FSG) as layer 104′, and silicon nitride as layer 102′, and with the exception of the interlayer insulating film including a third kind of an insulating layer under the second kind of the insulating layer 104′, the third kind of the insulating layer having etching characteristics different from the second kind of the insulating layer.

Tsai et al. teaches a semiconductor device that includes a dual damascene structure and further including a layer 206 of silicon nitride, an undoped oxide layer 208 overlying the layer 206 of silicon nitride, and a layer 210 of fluorosilicate glass(FSG) overlying the layer 208; wherein the undoped oxide layer 208 is underlying the fluorosilicate glass layer 210 and overlying the silicon nitride layer 206, and the USG layer 208 has a thickness thinner than a first depth, for the disclosed intended purpose of changing the surface condition between the stop layer 206 and the FSG layer 210, and eliminating the surface dependence between the stop layer 206 and the FSG layer 210, and resulting in a FSG layer 210 having a uniform thickness and improved reliability (Col. 3, ll. 42-54).

Thus, it would have been obvious to one of ordinary skill in the art to form a third kind of insulating layer under the second kind of insulating layer as Tsai et al. teaches for the disclosed intended purpose of obtaining a second insulating layer having a uniform thickness and improved reliability, furthermore regarding the limitation of the third insulating layer having etch characteristics different from the second insulating layer, it is noted that the selectivity in etching characteristics will depend in the etchant chemistry utilized, and that as the materials of the second and third insulating materials are different, the materials will have different etching characteristics.

Thus, it would have been obvious to one of ordinary skill in the art to use a contact hole having a gradual increase toward an upper level as Huang et al. teaches that this is well known and conventional in the art, and an inherent result of the gradual increase is a conformal barrier layer that aids in the adhesion of the embedded conductive layer while preventing the diffusion of the embedded layer.

Regarding claim 5, Uglow et al. as modified by Huang et al., teaches the second kind of the insulating layer is capable of functioning as an etch stopper while the first kind of the insulating layer is etched, and the contact hole has a substantially same cross sectional shape from a bottom surface of the second kind of the insulating layer to the surface of the conductive region.

Regarding claims 19-24, Uglow et al. as modified by Huang et al. discloses a shoulder at the upper portion which extends from the bottom surface into the second

kind of the insulating layer, wherein the shoulder is smoothly continuous with the bottom surface, and formed by the etching from above and from the contact hole. Furthermore, it would have been within the scope of one of ordinary skill in the art at the time the invention was made that formation of the shoulder is a result of the etching process used and that such a structure would result in a better conformal deposition of the conductive layers than when sharp edges and corners are present in the structure.

Regarding claims 25 and 26, Uglow et al. as modified by Huang et al., discloses that the first and second kinds of insulating layers include one or more of silicon dioxide, fluorinated silica glass, silicon nitride, and carbon doped oxide. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use any of the materials taught by Uglow et al. as long as the layers are of different materials as taught by Uglow et al., since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

4. Claims 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uglow et al. as modified by Huang et al. as applied to claims 1 and 7 above, and further in view of Huang (U. S. Pat. 6,096,595).

Uglow et al. as modified by Huang et al. above discloses the claimed invention including the insulating etch stopper film comprising one of silicon nitride and silicon carbide, the insulating layer comprising silicon oxide, the silicon oxide including TEOS oxide, FLUOROSILICATE (FSG), and the like, and with the exception of the underlie

comprising a silicon substrate formed with shallow trench isolation defining active regions, CMOS transistors formed in the active regions, each transistor having an insulated gate electrode on the active region, and source/drain regions formed in the active region on both sides of the gate electrode.

Huang discloses a semiconductor device that comprises a dual damascene structure in contact with an underlie, wherein the underlie comprises a silicon substrate formed with shallow trench isolation defining active regions, CMOS transistors formed in the active regions, each transistor having an insulated gate electrode on the active region, and source/drain regions formed in the active region on both sides of the gate electrode, wherein the underlie further comprises lower insulating layers formed on the silicon substrate covering the gate electrodes and the source/drain regions, and at least one wiring layer embedded in the lower insulating layer, and wherein the structure is taught as a conventional integrated circuit device and the damascene structure is in contact to the underlie for the disclosed intended purpose of interconnecting the structure to other areas of the circuit.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the dual damascene structure of Uglow et al. as modified by Huang et al. in an integrated circuit structure like the one taught by Huang for the purpose of interconnecting the structure to other areas of the circuit.

Response to Arguments

5. Applicant's arguments with respect to claims 1-7, and 19-30 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ginette Peralta whose telephone number is (703)305-7722. The examiner can normally be reached on Monday to Friday 8:00 AM- 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703)308-49188-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

GP
July 14, 2003

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800